

TO SIGNAL LINES

FIG. 1

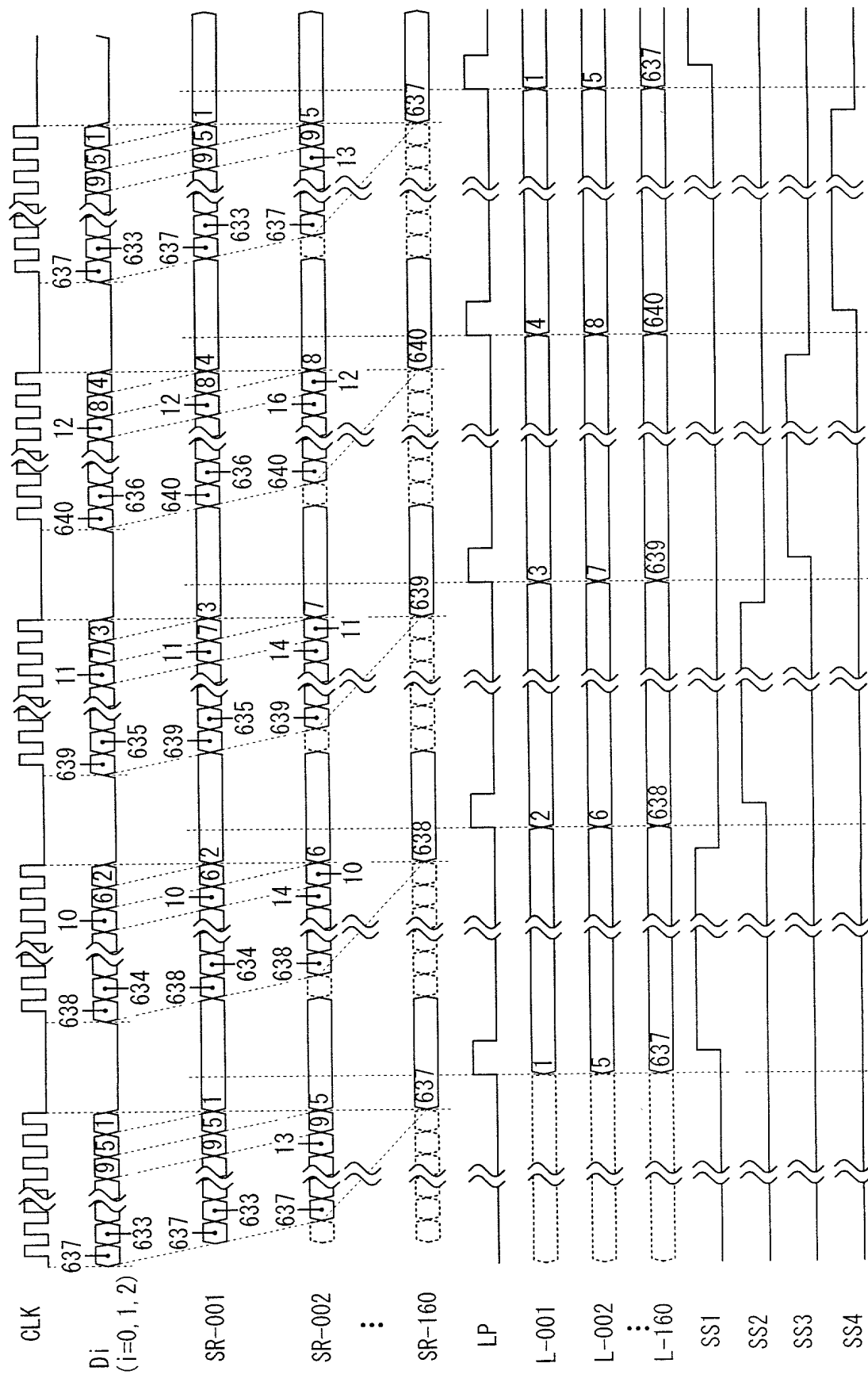
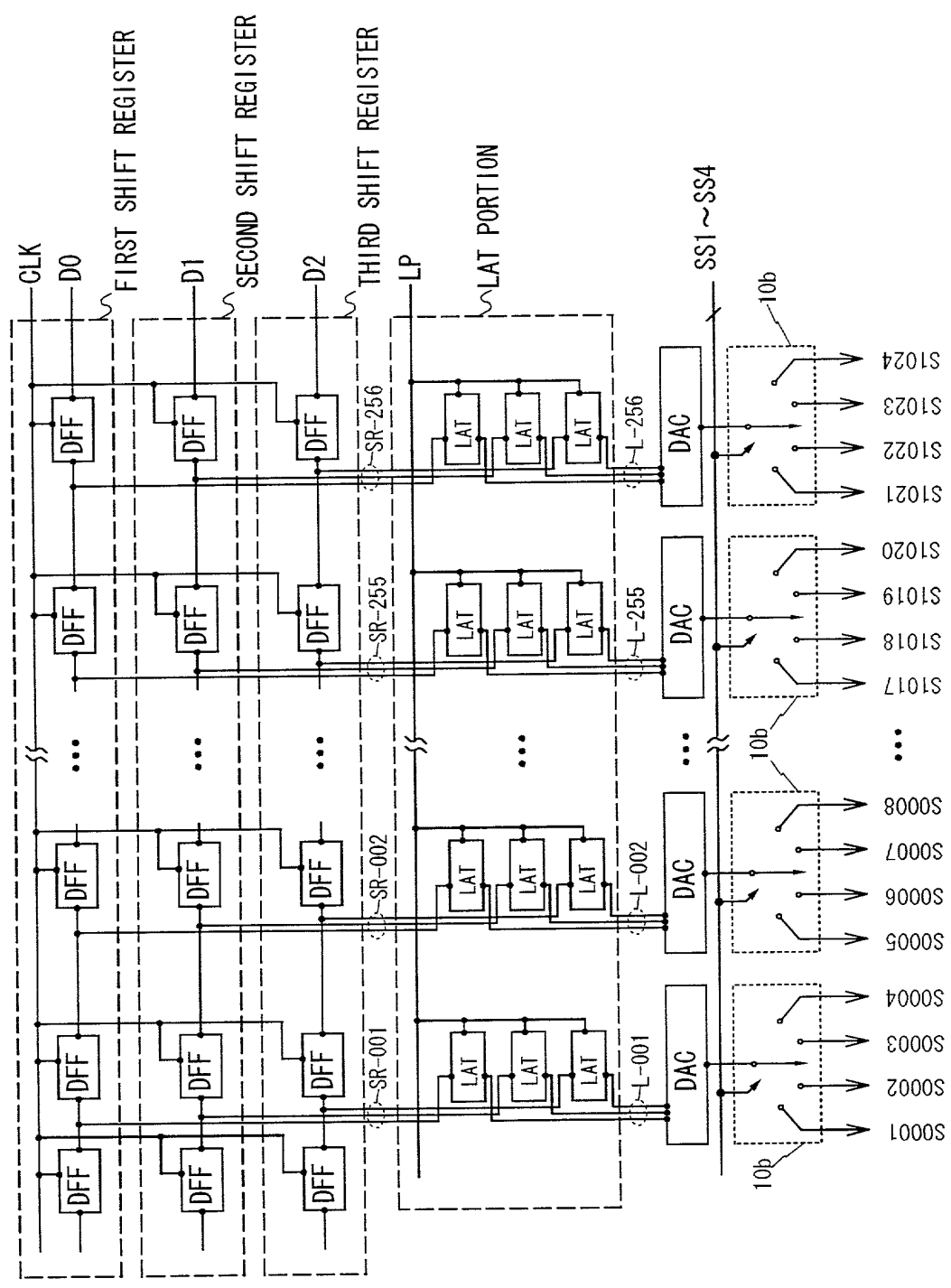


FIG. 2

FIG. 3 is a block diagram of a digital-to-analog converter (DAC) circuit. The circuit is organized into three main sections: a shift register section, a DAC section, and a signal output section. The shift register section consists of three shift registers (FIRST SHIFT REGISTER, SECOND SHIFT REGISTER, and THIRD SHIFT REGISTER) and a LAT PORTION. The shift registers are connected to a common clock (CLK) and data inputs (D0, D1, D2). The LAT PORTION is connected to the outputs of the shift registers and to a common output line (SS1~SS4). The DAC section contains four DAC blocks (DAC1, DAC2, DAC3, DAC4) which are connected to the outputs of the shift registers and the LAT PORTION. The signal output section shows the DAC outputs connected to a common output line (SS1~SS4) and then to a set of signal lines (S0001, S0002, S0003, S0004, S0005, S0006, S0007, S0008, S1017, S1018, S1019, S1020, S1021, S1022, S1023, S1024). The signal lines are connected to a set of switches (10b) which are controlled by a common output line (SS1~SS4). The switches are connected to a common output line (SS1~SS4) and then to a set of signal lines (S0001, S0002, S0003, S0004, S0005, S0006, S0007, S0008, S1017, S1018, S1019, S1020, S1021, S1022, S1023, S1024).

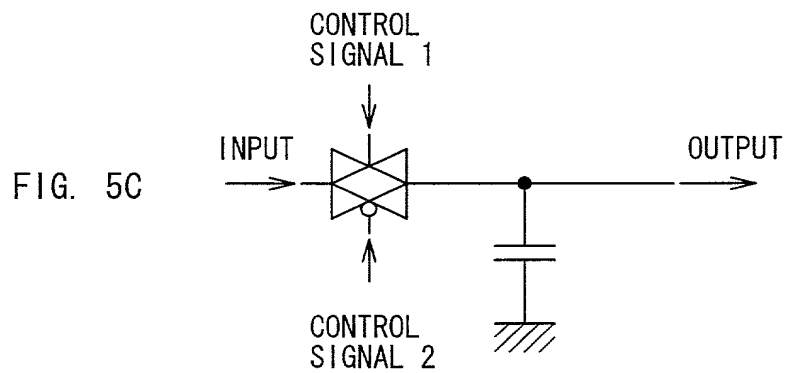
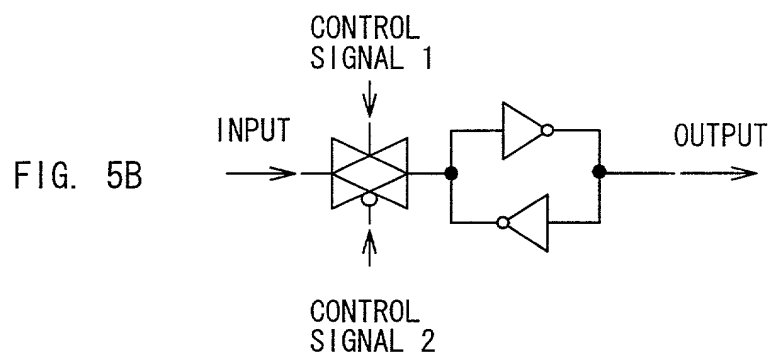
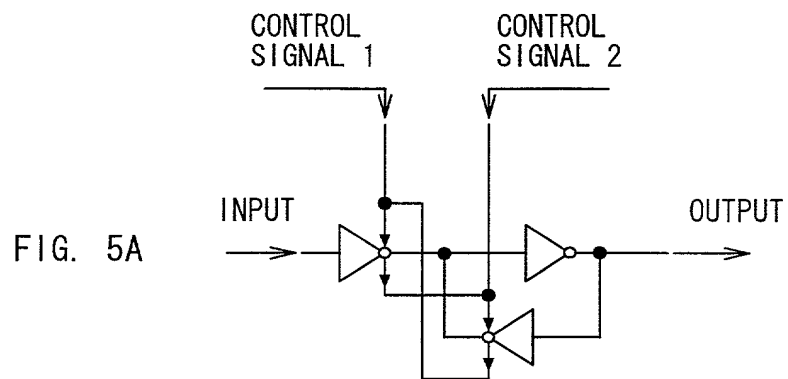


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FIG. 3



FIG. 4



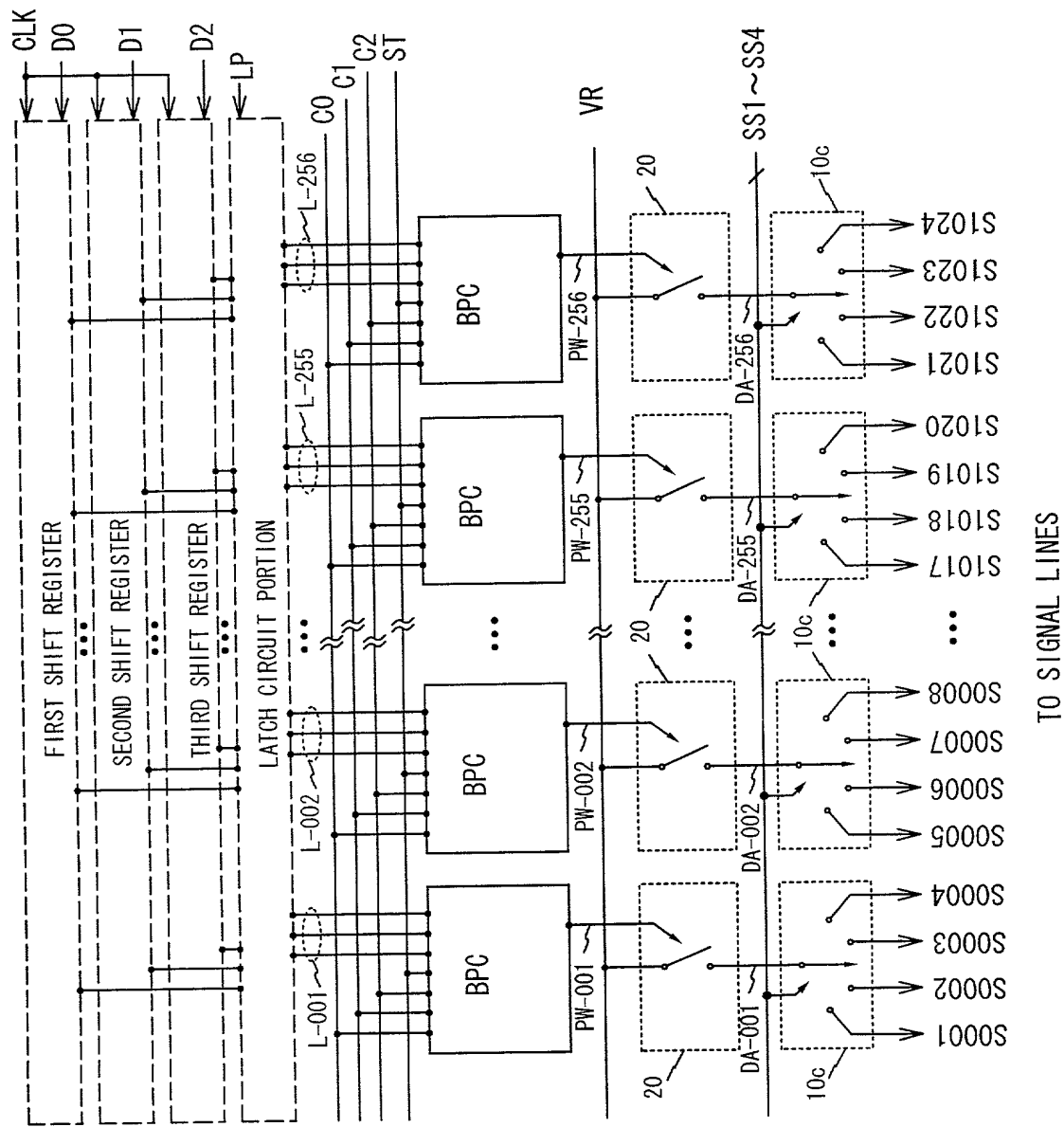


FIG. 6

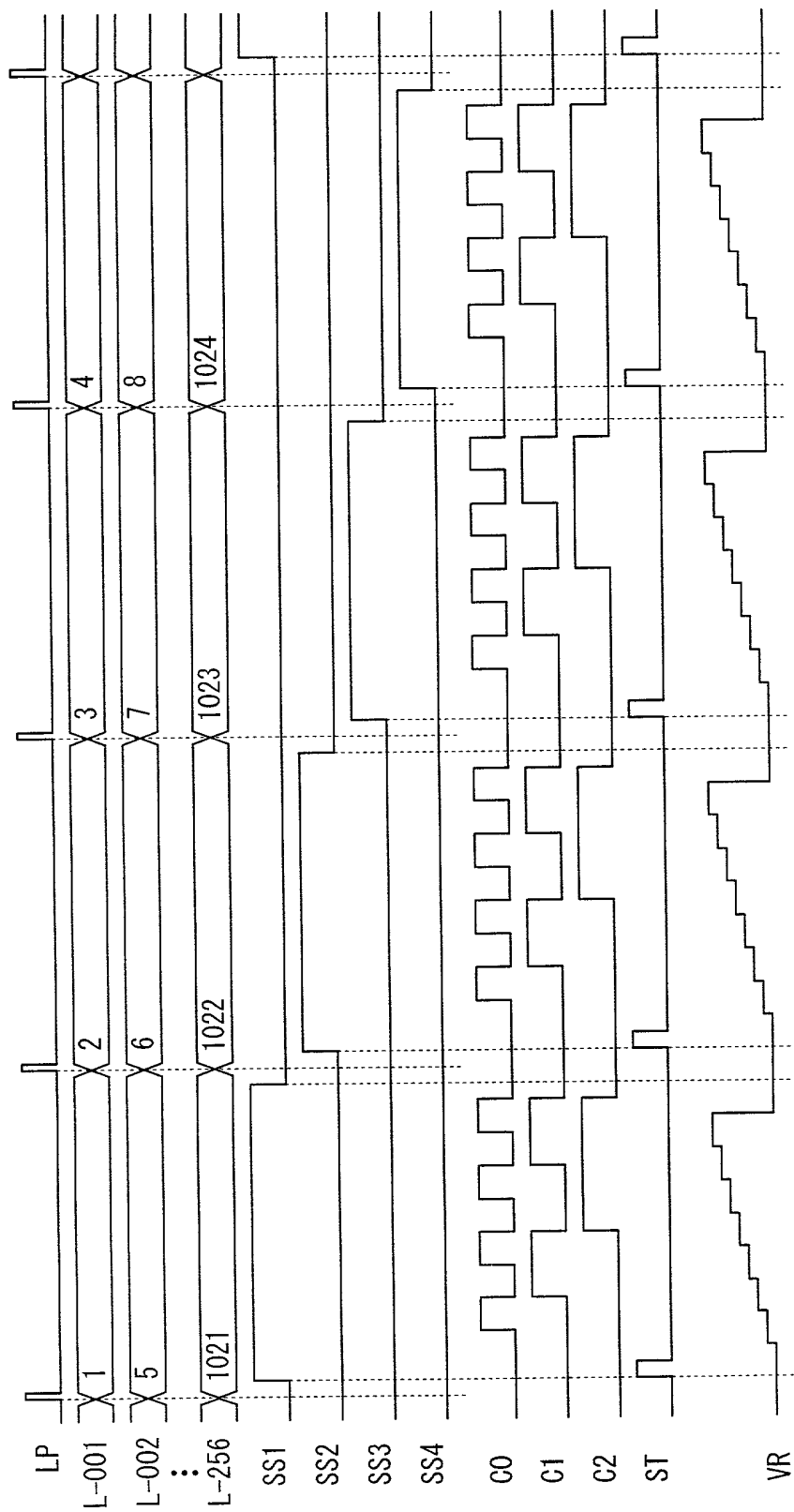


FIG. 7

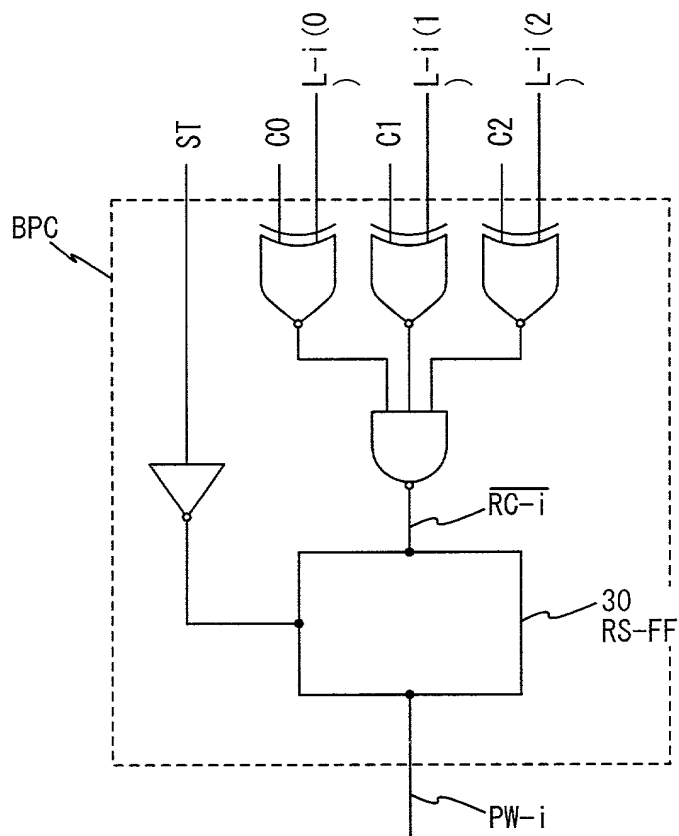


FIG. 8



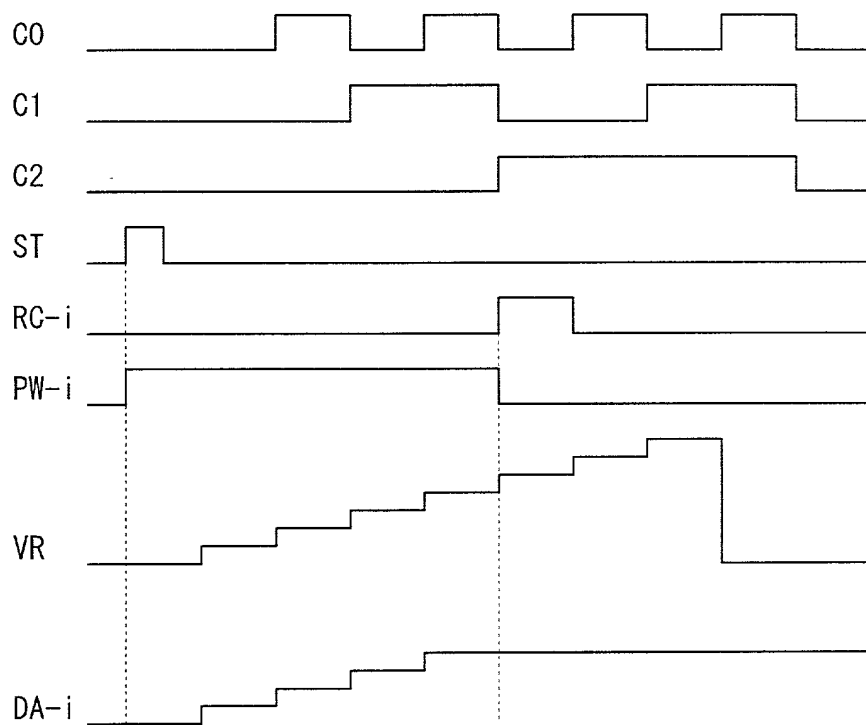


FIG. 9



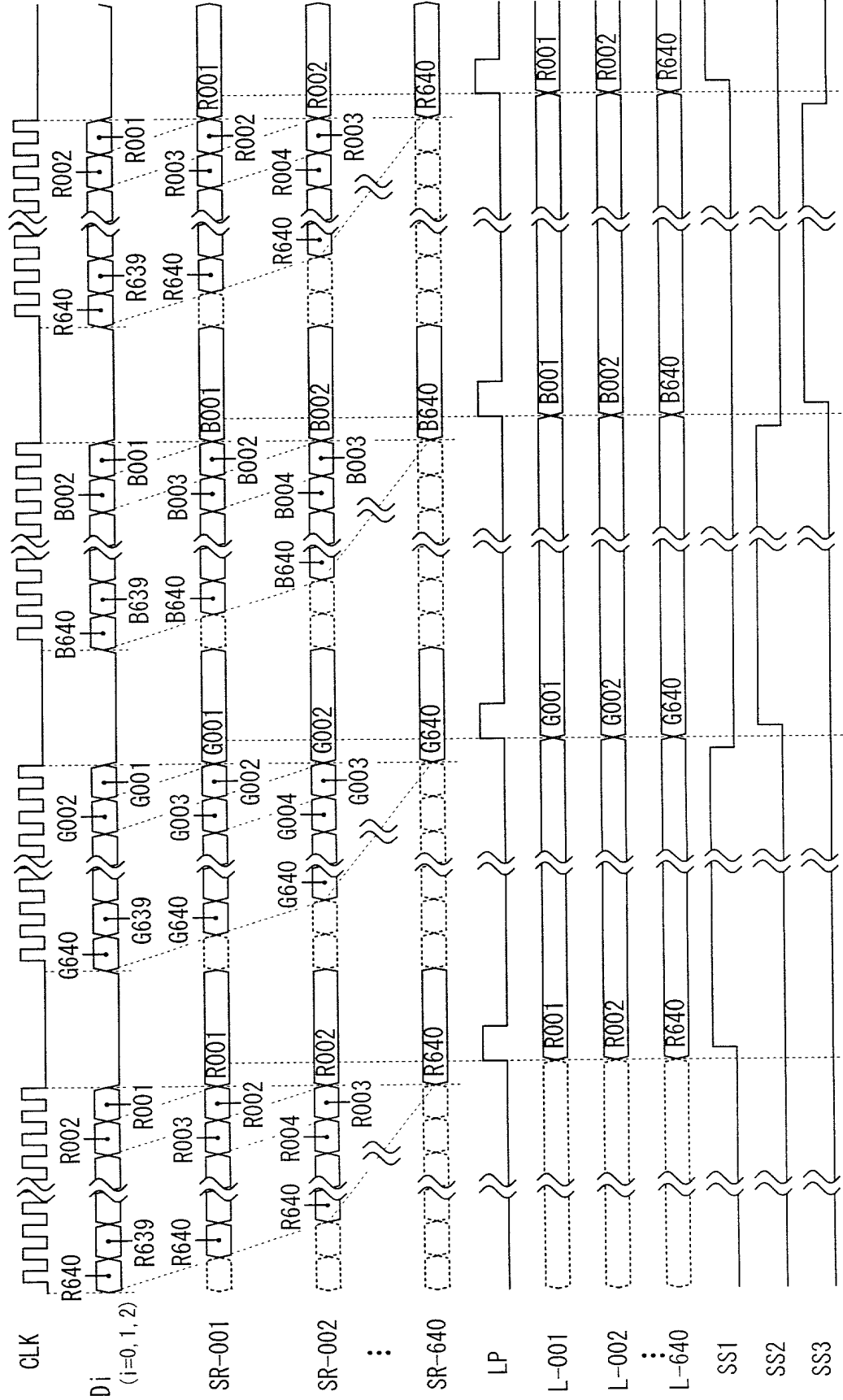


FIG. 11

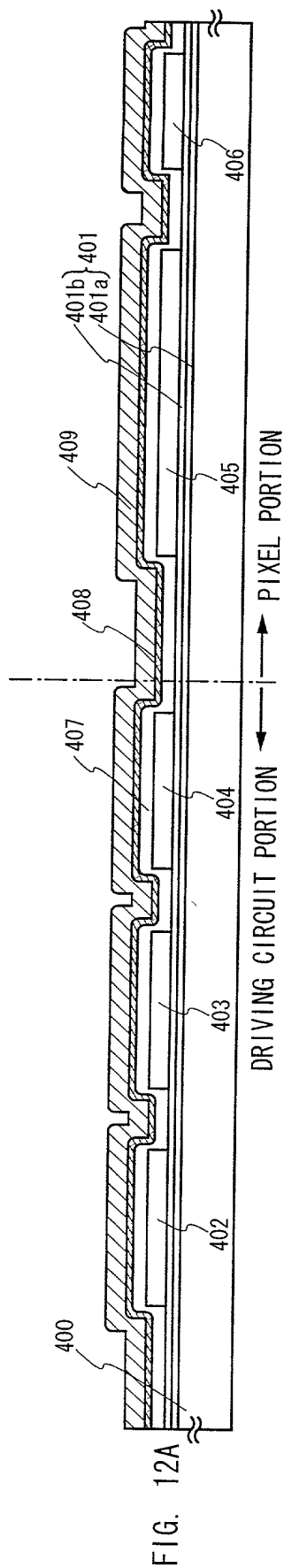


FIG. 12A

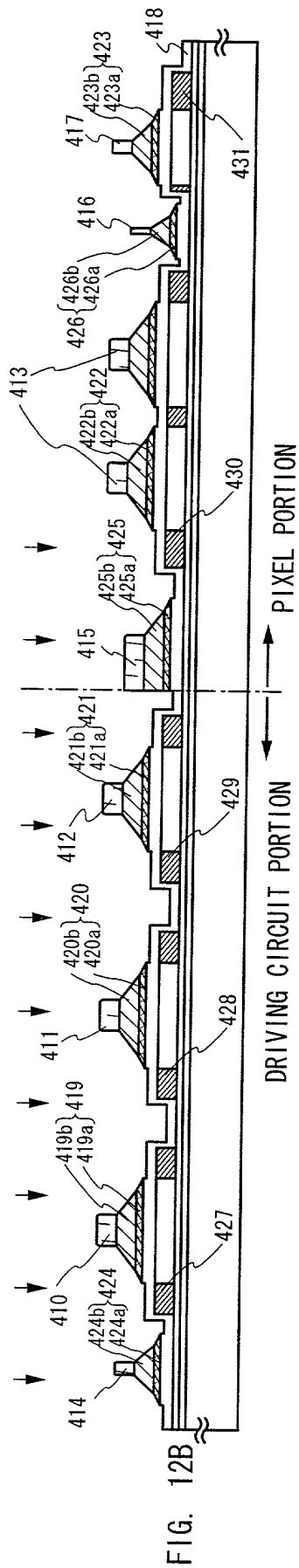


FIG.

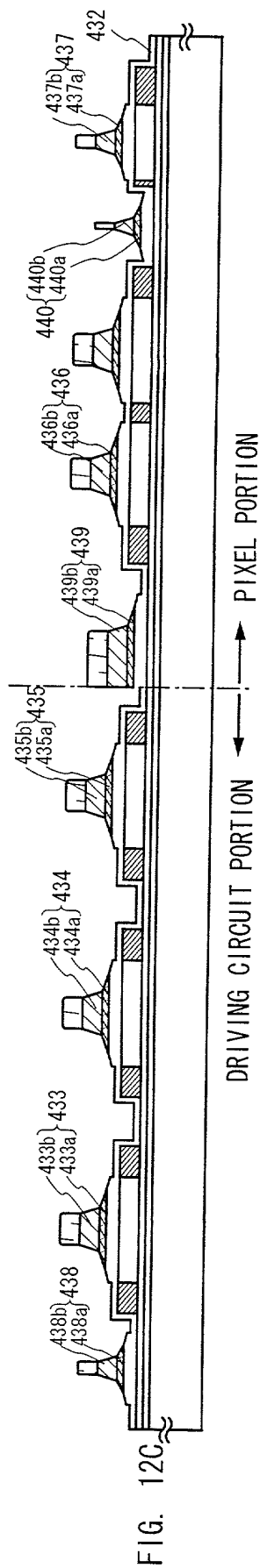


FIG. 12C

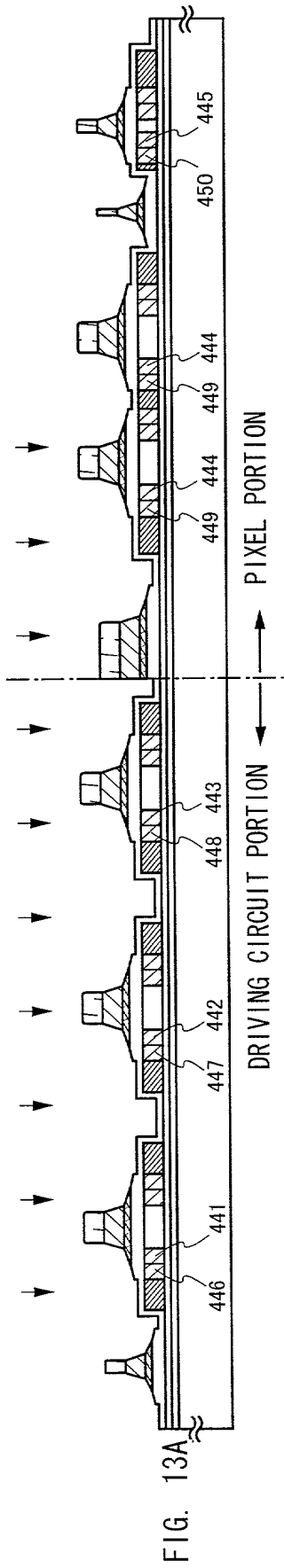


FIG. 13A

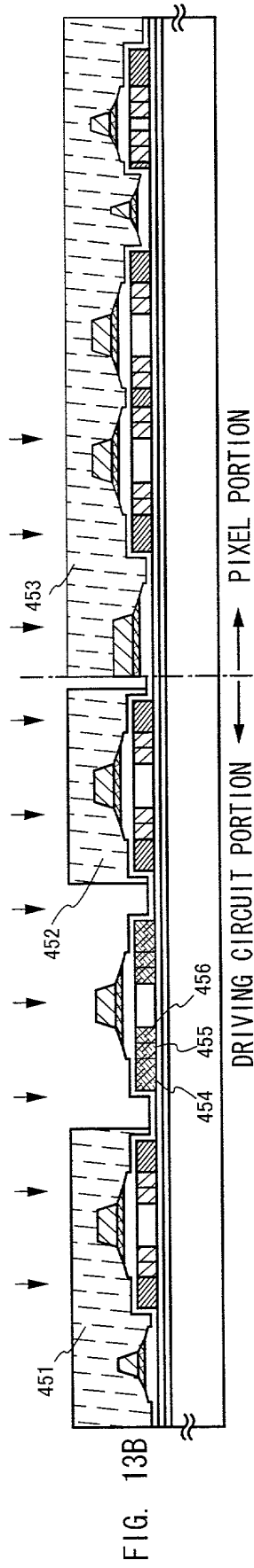


FIG. 13B

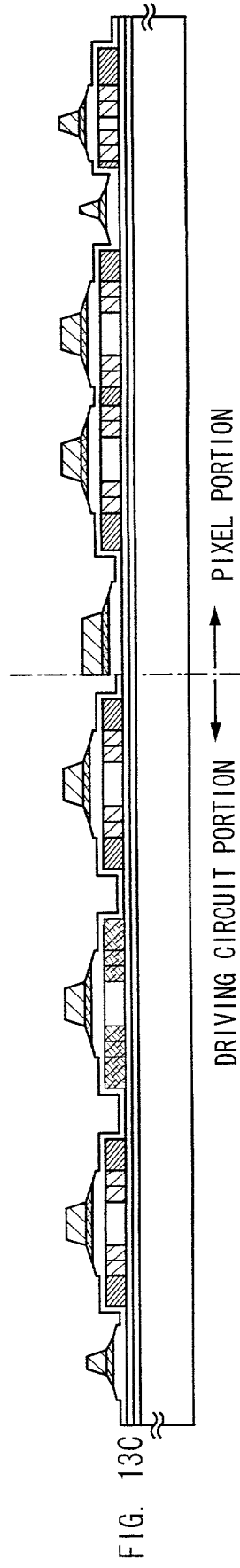


FIG. 13C

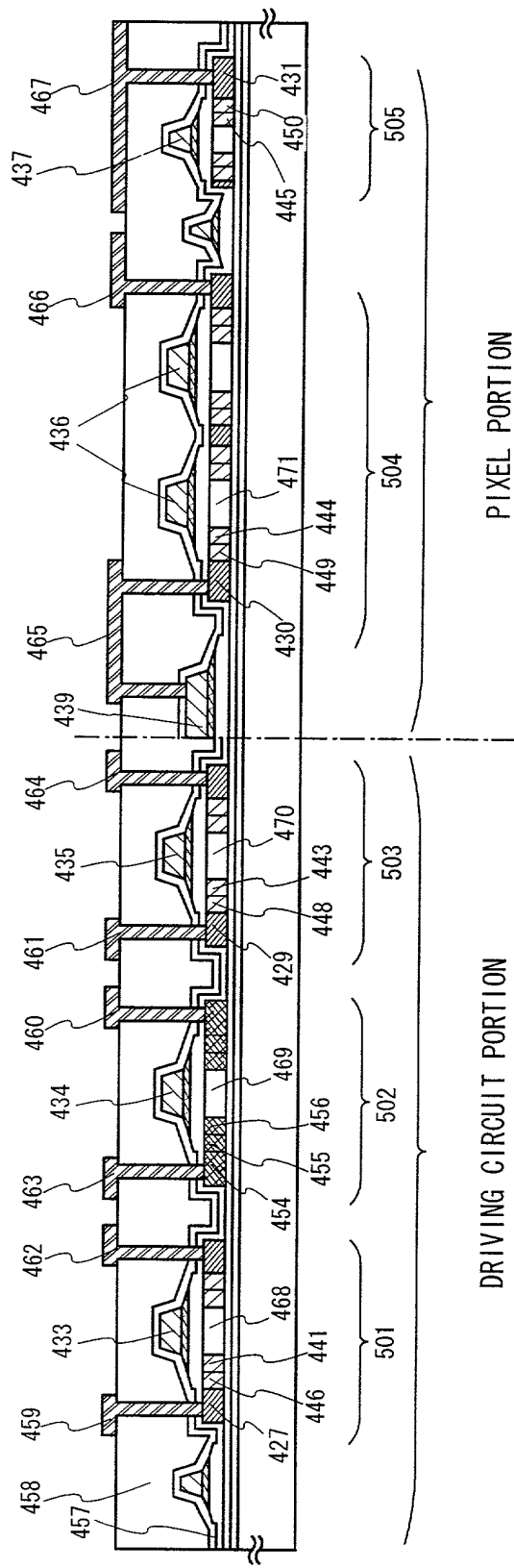


FIG. 14

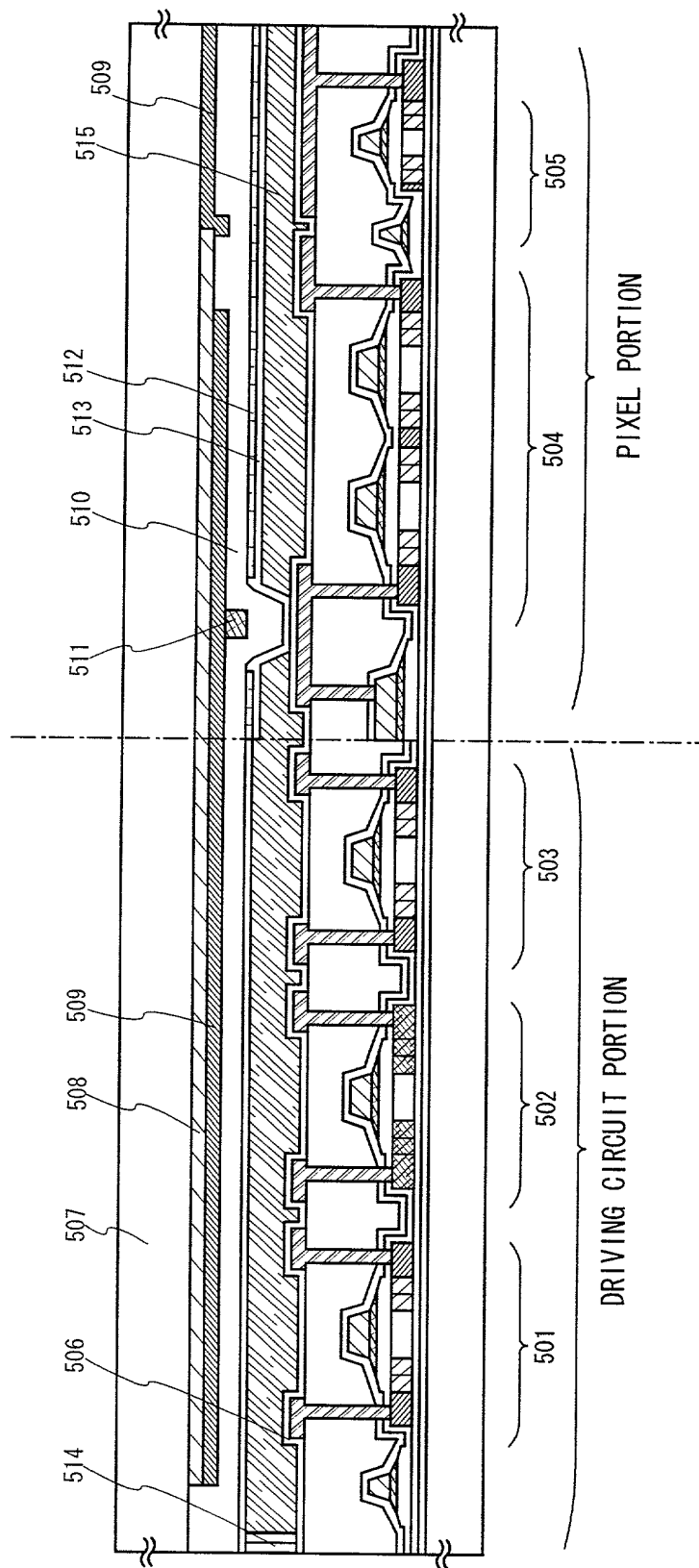
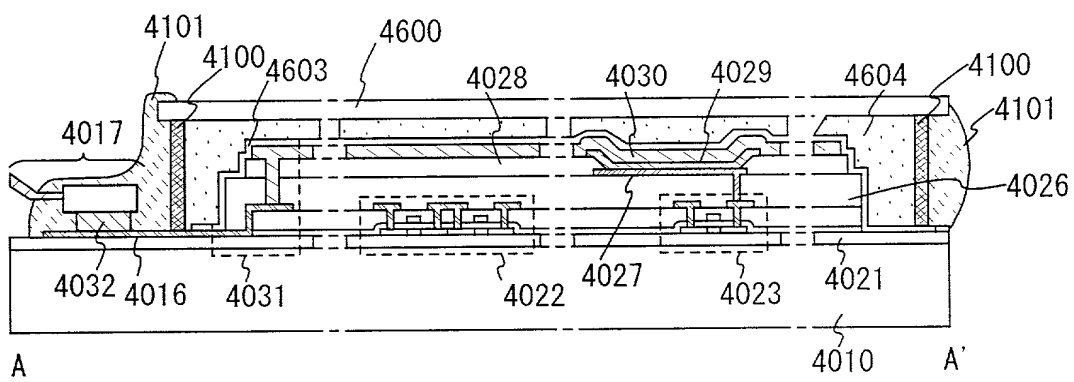
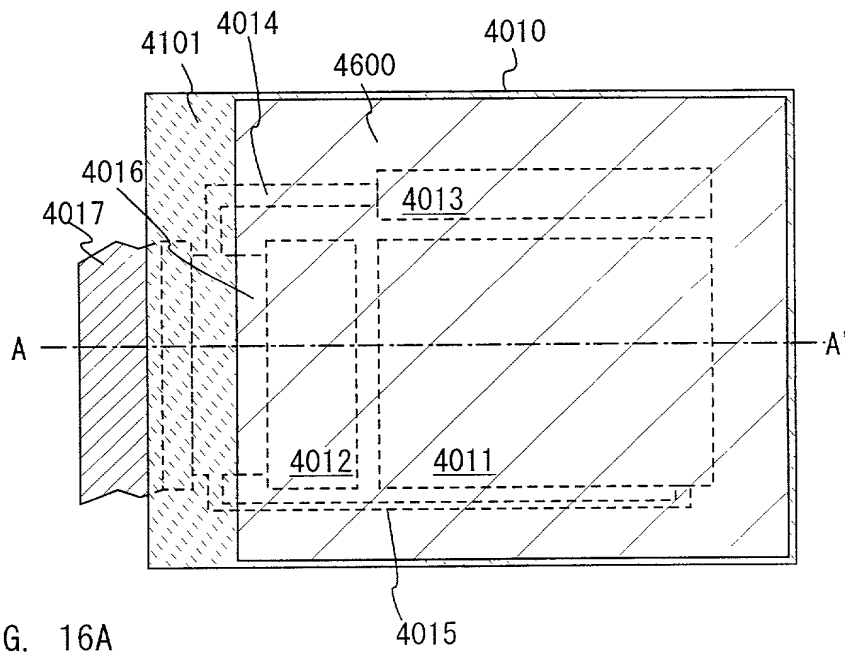


FIG. 15





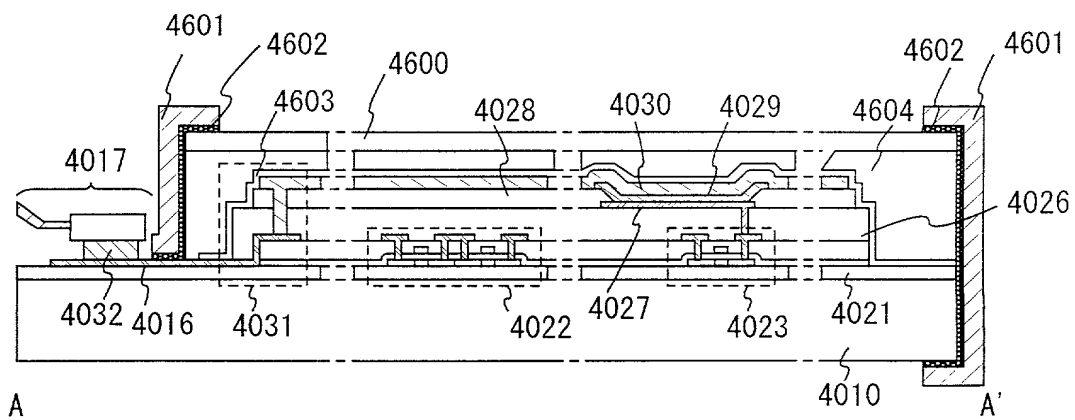
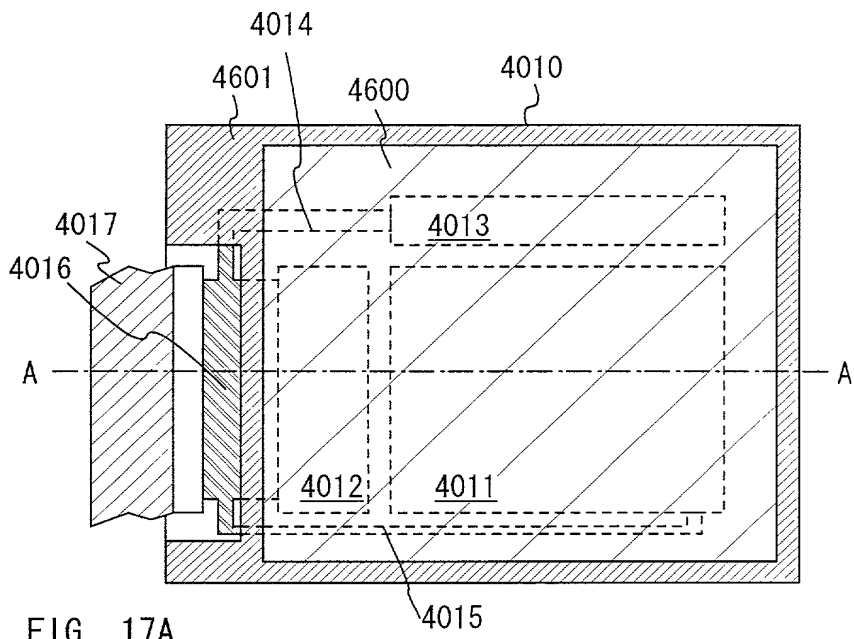


FIG. 18 is a cross-sectional view of a light emitting device in a direction of light emission.

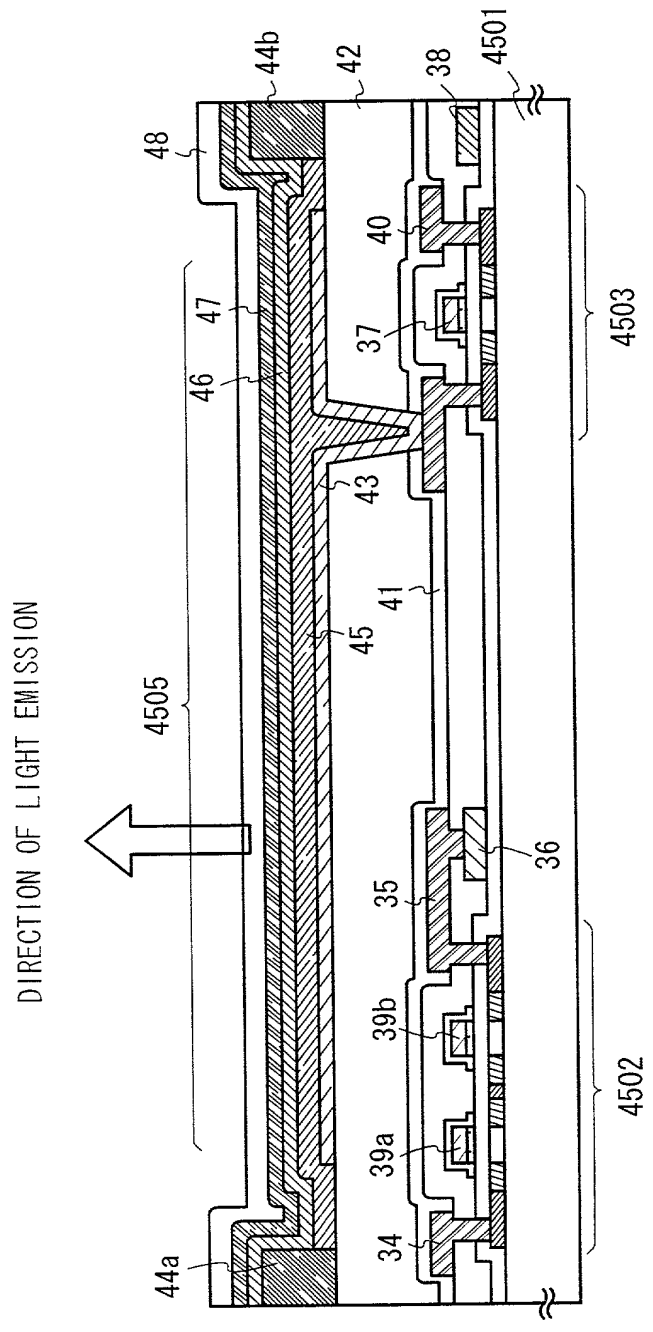


FIG. 18

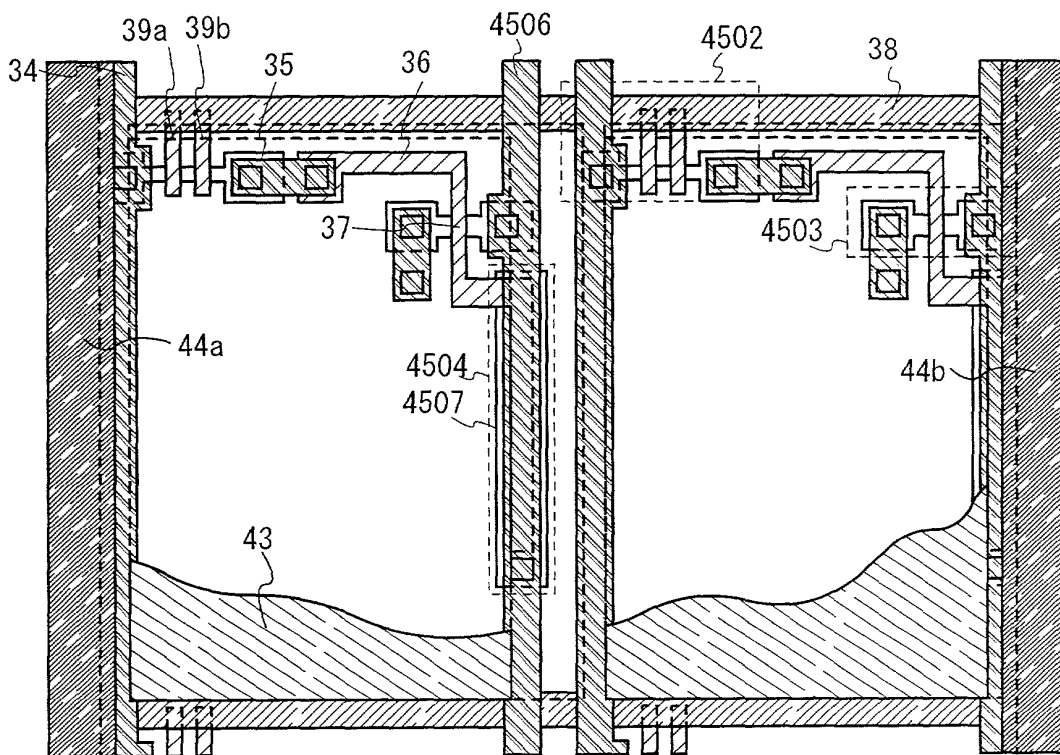


FIG. 19A

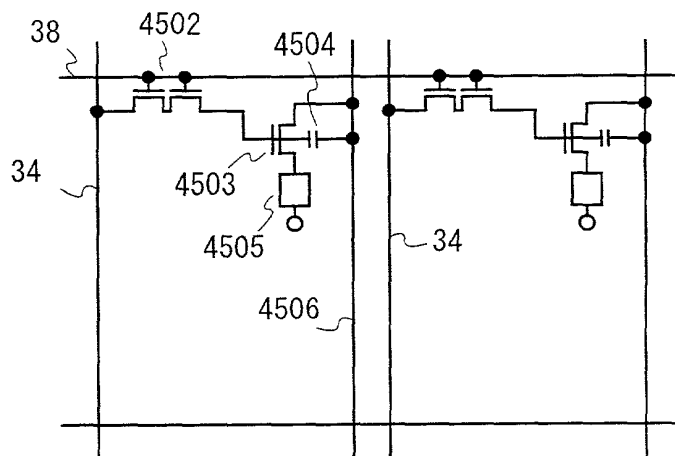


FIG. 19B

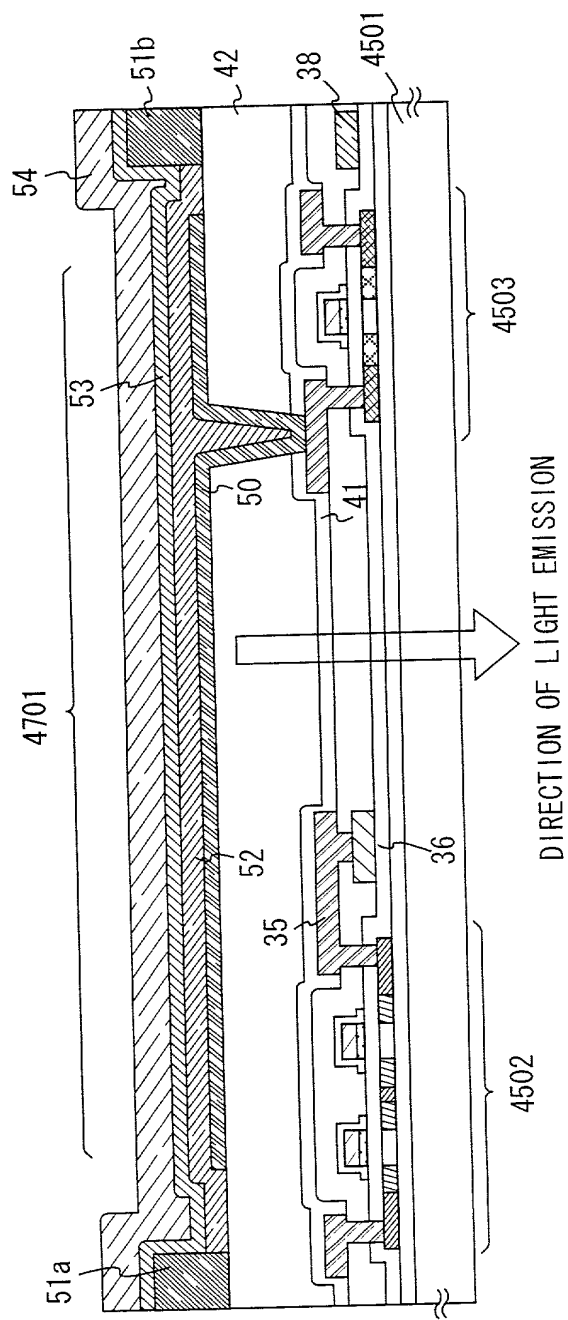
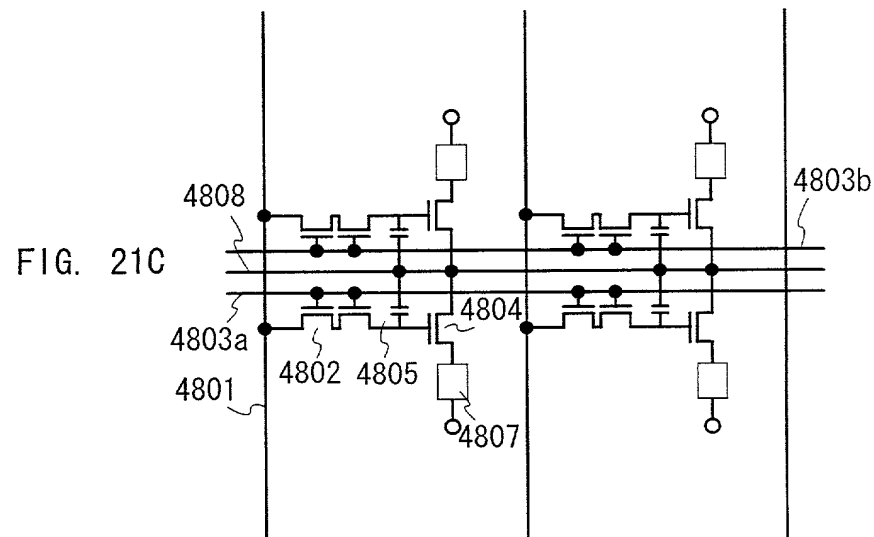
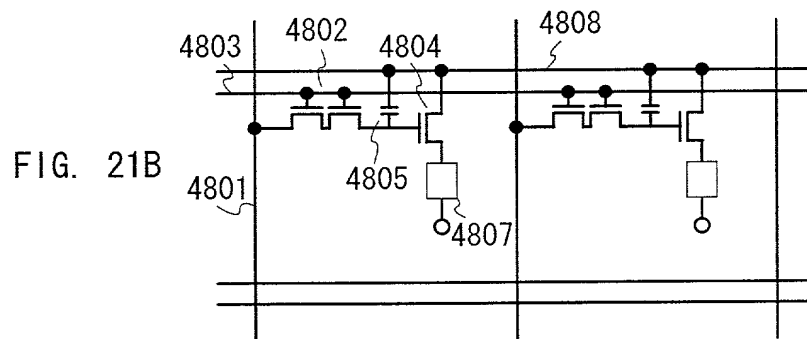
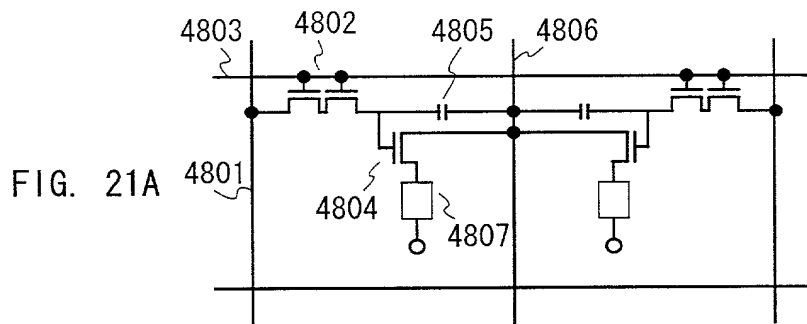


FIG. 20



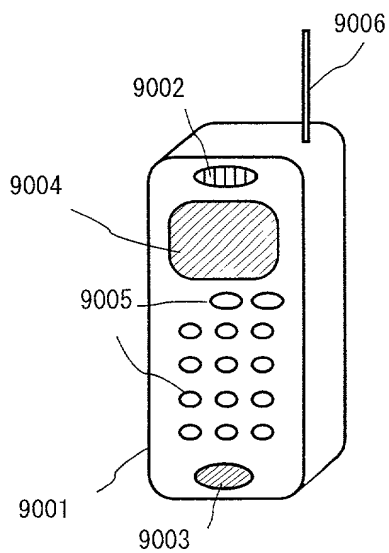


FIG. 22A

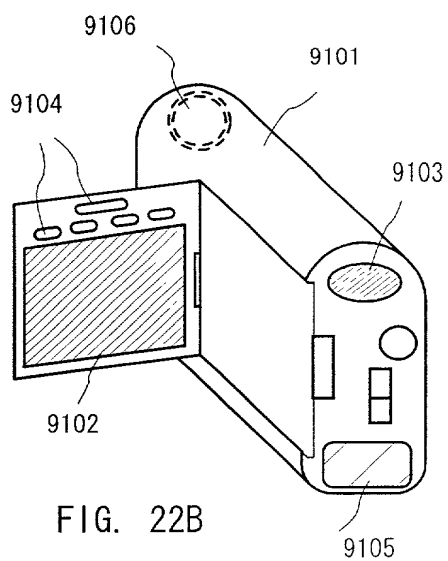


FIG. 22B

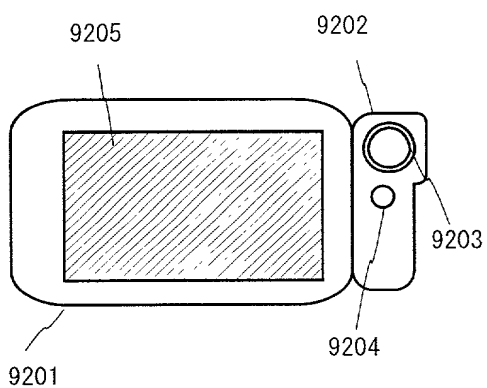


FIG. 22C

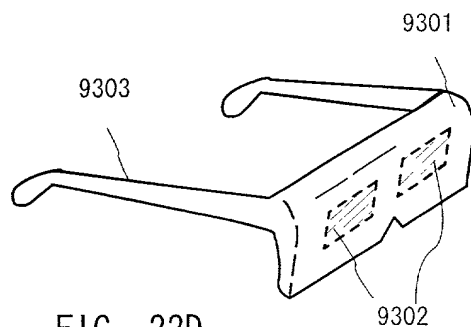


FIG. 22D

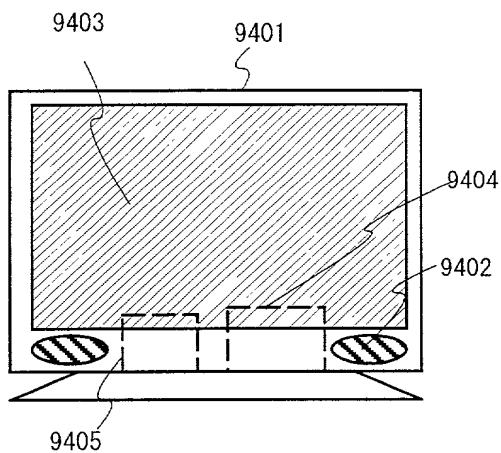


FIG. 22E

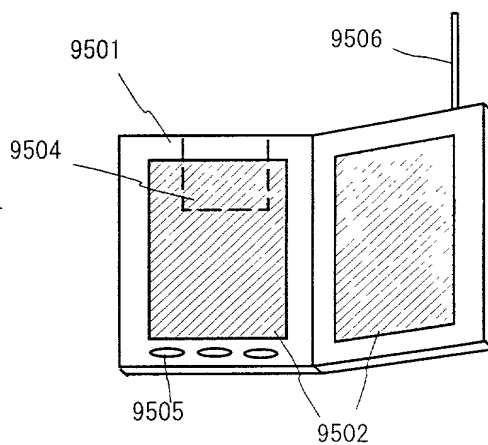


FIG. 22F

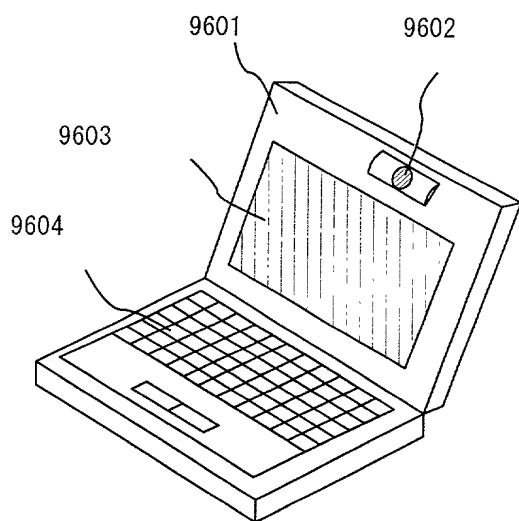


FIG. 23A

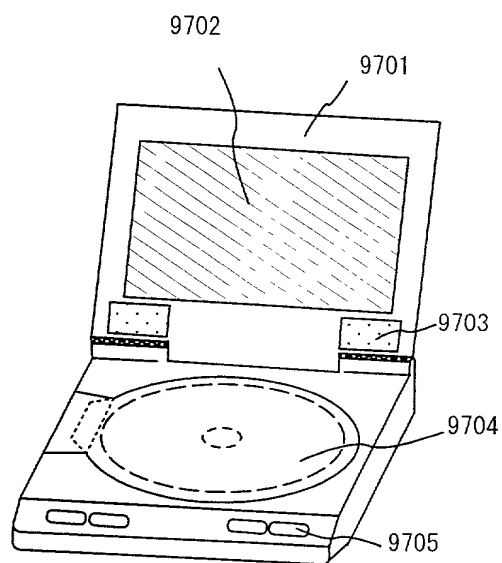


FIG. 23B

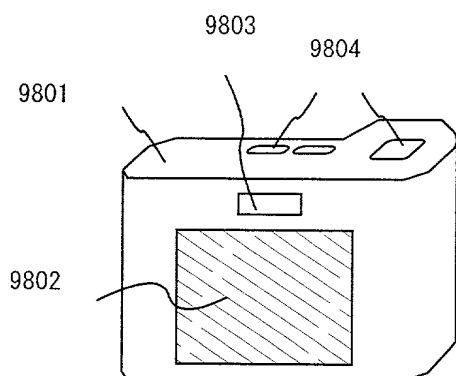


FIG. 23C

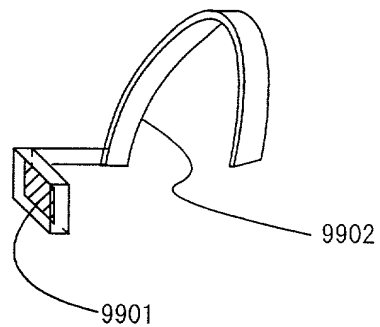


FIG. 23D

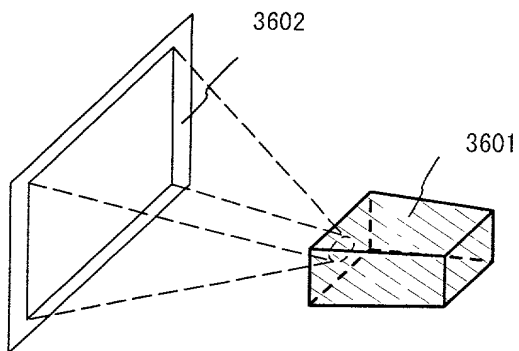


FIG. 24A

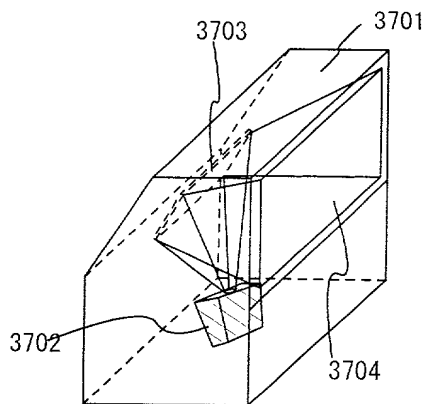


FIG. 24B

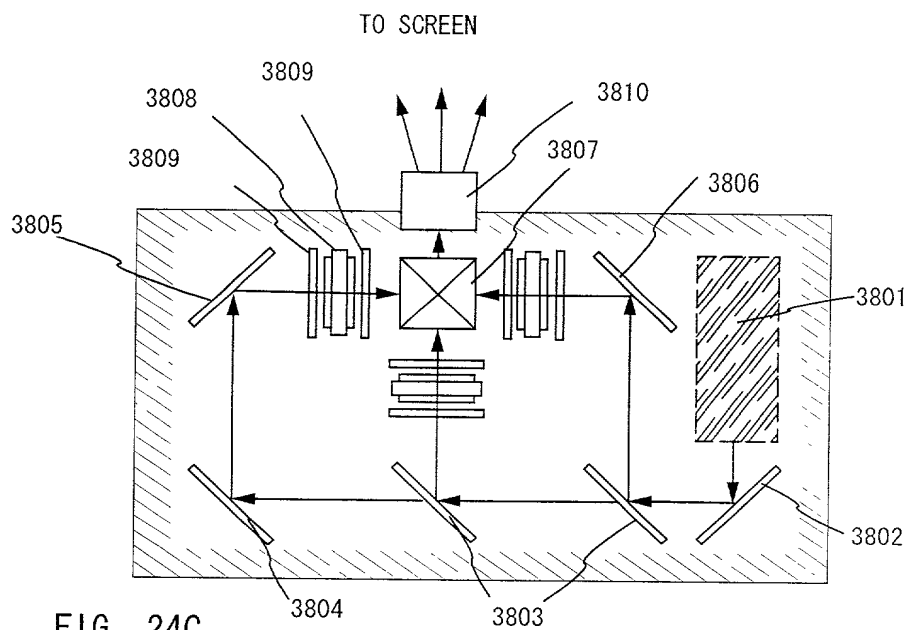


FIG. 24C

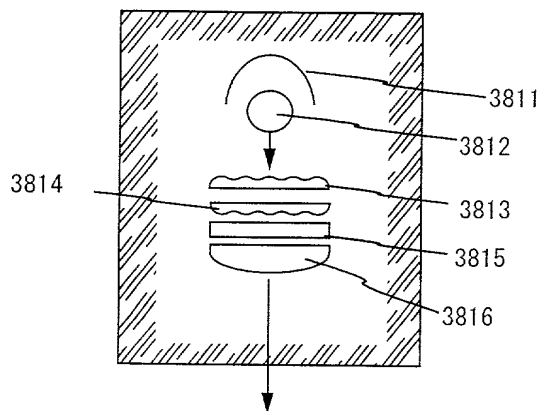


FIG. 24D



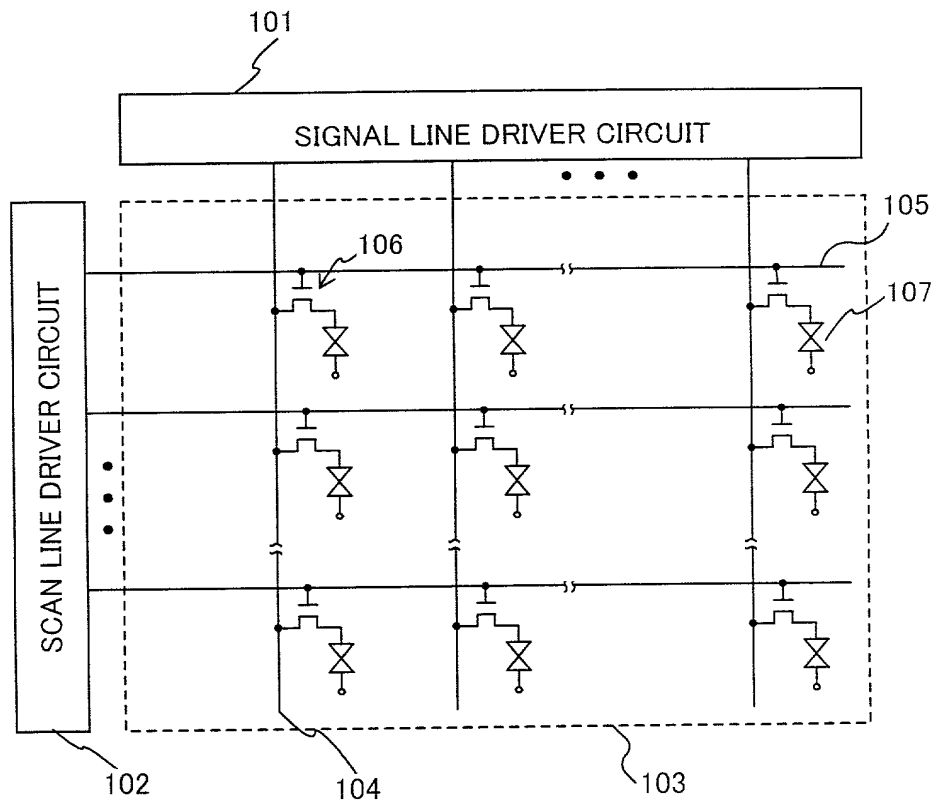


FIG. 25

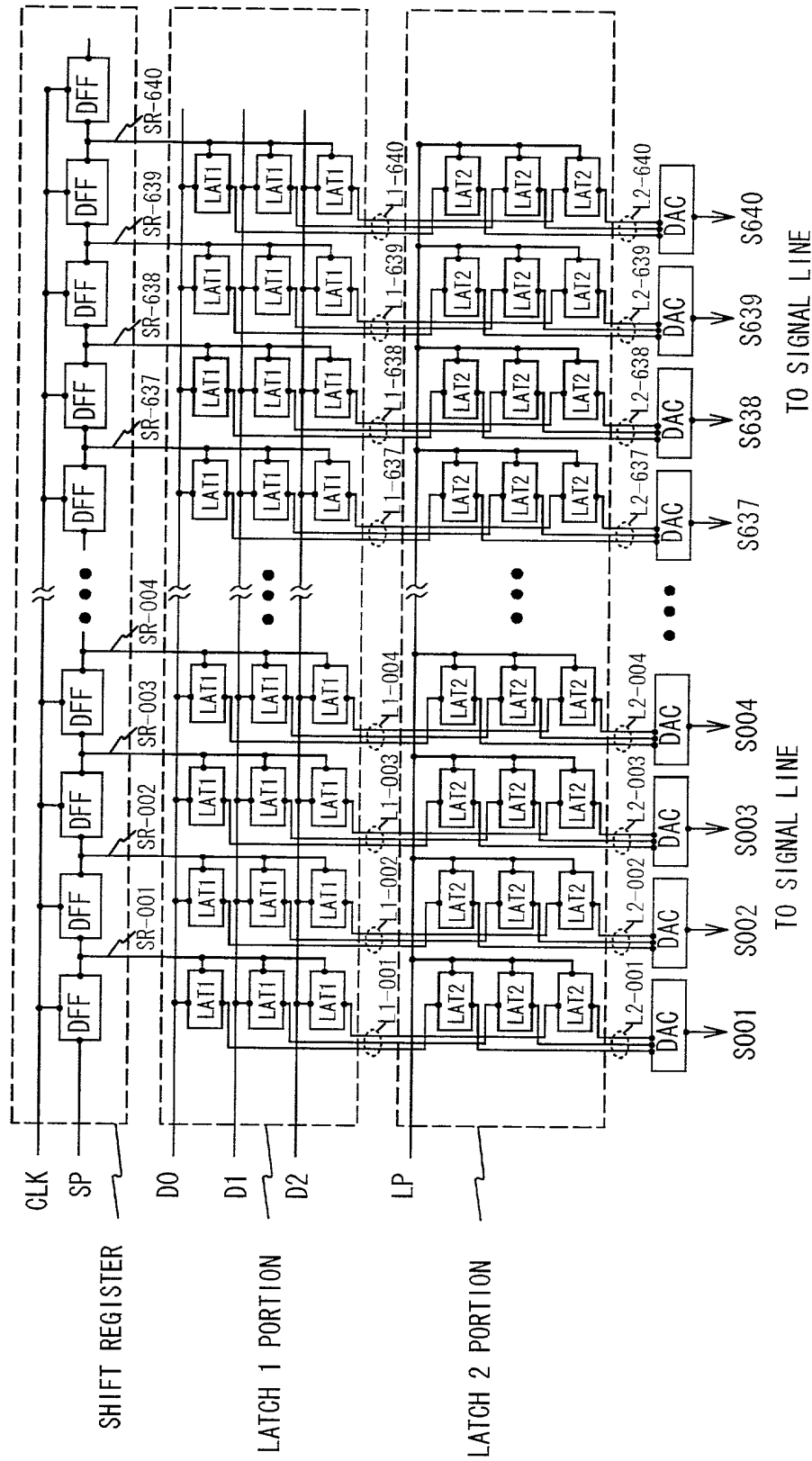


FIG. 26

FIG. 27